ABSTRACT OF THE INVENTION

An isolation-less, contact-less nonvolatile memory array has a plurality of memory cells each with a floating gate for the storage of charges thereon, arranged in a plurality of rows and columns. Each memory cell can be of a number of different types. All the bit lines and source lines of the various embodiments are buried and are contact-less. In a first embodiment, each cell can be represented by a stacked gate floating gate transistor coupled to a separate assist transistor. The entire array can be planar; or in a preferred embodiment each of the floating gate transistors is in a trench; or each of the assist transistors is in a trench. In a second embodiment, each cell can be represented by a stacked gate floating gate transistor with the transistor in a trench. In a third embodiment, each cell can be represented by two stacked gate floating gate transistors coupled to a separate assist transistor, positioned between the two stacked gate floating gate transistors. The entire array can be planar; or in a preferred embodiment each of the floating gate transistors is in a trench; or each of the assist transistors is in a trench. Novel methods to manufacture the arrays and methods to program, erase, and read each of these embodiments of the memory cells is disclosed.